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FOUR PARAMETER PULSE HEIGHT ANALYZER

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NASA — GODDARD SPACE FLIGHT CENTER

GREENBELT, MARYLAND

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FOUR PARAMETER PULSE HEIGHT ANALYZER

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INTRODUCTION

The Mark 9 Wide Dynamic Range A to D Converter and Readout System (ADCR-9) is a modified Mark 6 system (see GSFC X-611-64-183). The modifications consist of addition of charge amplifiers at the inputs of existing channels A, B, and C and the addition of a fourth "D" channel. The output of the fourth channel detector is analyzed (whenever A and B channel outputs are coincident) to determine whether its total charge is less than level D1, between level D1 and D2 or greater than level D2. The level of D is indicated by the digital outputs on tape track "8-initial" and tape track "8-delayed". The indexing bits normally connected to tape track "8-initial" and tape track "8-delayed" in the ADCR Mark 6 system are disconnected from this track in the Mark 9 system.

CHANNEL D OPERATION

Figure 1 is a block diagram of the D channel in the ADCR Mark 9. Output charge pulses from D detector, obtained as a result of incident cosmic rays, are fed to the charge amplifier. The charge amplifier integrates and yields a voltage output pulse whose peak amplitude is proportional to the total charge in the input pulse. This voltage pulse is fed directly into threshold detector D2 and through the voltage amplifier to threshold detector D1. Threshold detectors D1 and D2 yield a 2.5 microsecond output pulse whenever the input charge level exceeds D1 and D2 respectively. Scaler D1, normally in the reset state, is triggered to the set state when a threshold detector D1 output pulse and an A and B coincidence pulse are applied to the D1 AND gate. Similarly, scaler D2 is set when threshold detector D2 output pulse occurs simultaneously with the A and B coincidence pulse. The states of scalers D1 and D2 are read out, through the readout switch, onto magnetic tape track 8 initial readout and delayed readout respectively.

PHYSICAL LAYOUT

The ADCR Mark 9 system houses the A, B, C and D channel detectors and charge amplifiers in a package separate from the electronics package. The respective channels in each package are interconnected by a cable. This

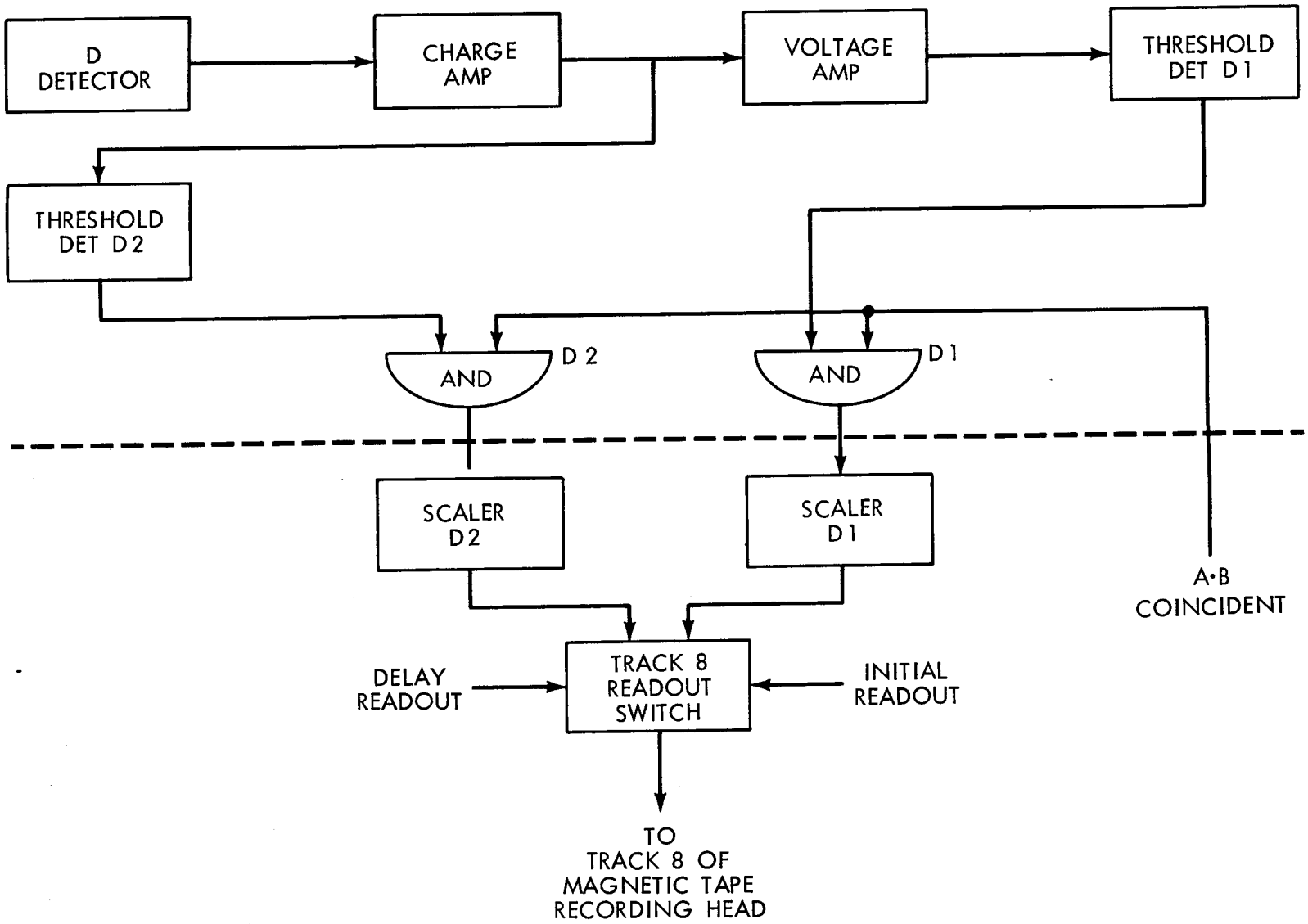


Figure 1. Channel D, ADCR Mark 9.

requires use of matching transformers at each end of the respective channel cable. The details of these transformer interconnections are given in the list of modifications below.

Channel D threshold detectors, gates and voltage amplifier are mounted on new board 7 as shown in Figure 2. Board 7 is mounted on the existing (ADCR-6) board 4. Figure 2 shows the interconnections of the circuits on board 7, the connections between board 7 and board 4 and the circuit modifications made to board 4. Details of these connections and modifications are given in the list of modifications below.

The A and B coincident signal pulse required by the D channel logic circuitry on board 7 is connected by an added co-ax cable from existing board 2 (ADCR-6) to the new board 7. Details of these connections are also given in the list of modifications below.

CIRCUIT DESIGN

Figure 3 is a schematic diagram of the charge amplifier. Transistors Q1, Q2 and Q3 form an operational amplifier. Capacitor C2 couples the operational amplifier output to the input, integrating the input charge. Thus the peak output voltage is proportional to the total input charge. The value of capacitor C2 determines the amplifier sensitivity and may be adjusted between 5 picofarads and 75 picofarads. Resistor R14 provides a discharge path for C2 controlling the fall time of the output signal. Transistor stage Q4 is an emitter follower which decouples the amplifier from the output. Transformer T1 is used to match the output impedance to the output cable.

Figure 4 is a schematic diagram of the voltage amplifier. This is a non-inverting bootstrap amplifier with the gain approximately equal to (R5 + R6)/R6. The gain is adjustable by use of a resistor in parallel with R5.

Figure 5 is a schematic diagram of the threshold detector and gate. Transistor stages Q1 and Q2, together with tunnel diodes CR1, CR2 and CR3 form a threshold detector-double pulse monostable circuit. This circuit is described in detail in GSFC Report X-711-65-435, "Low Power Nanosecond Pulse and Logic Circuits Using Tunnel Diodes," page 13. Whenever the input signal amplitude exceeds approximately 100 millivolts an output pulse of 2.5 microseconds width is obtained across R8, CR2 and CR3. Transistors Q3 and Q4 form an AND gate with the threshold detector output controlling Q3 and the A and B coincident pulse (2.0 microsecond width) controlling Q4. Thus an output is obtained at terminal 9 whenever a D channel input signal exceeds the threshold level and is coincident with A and B.

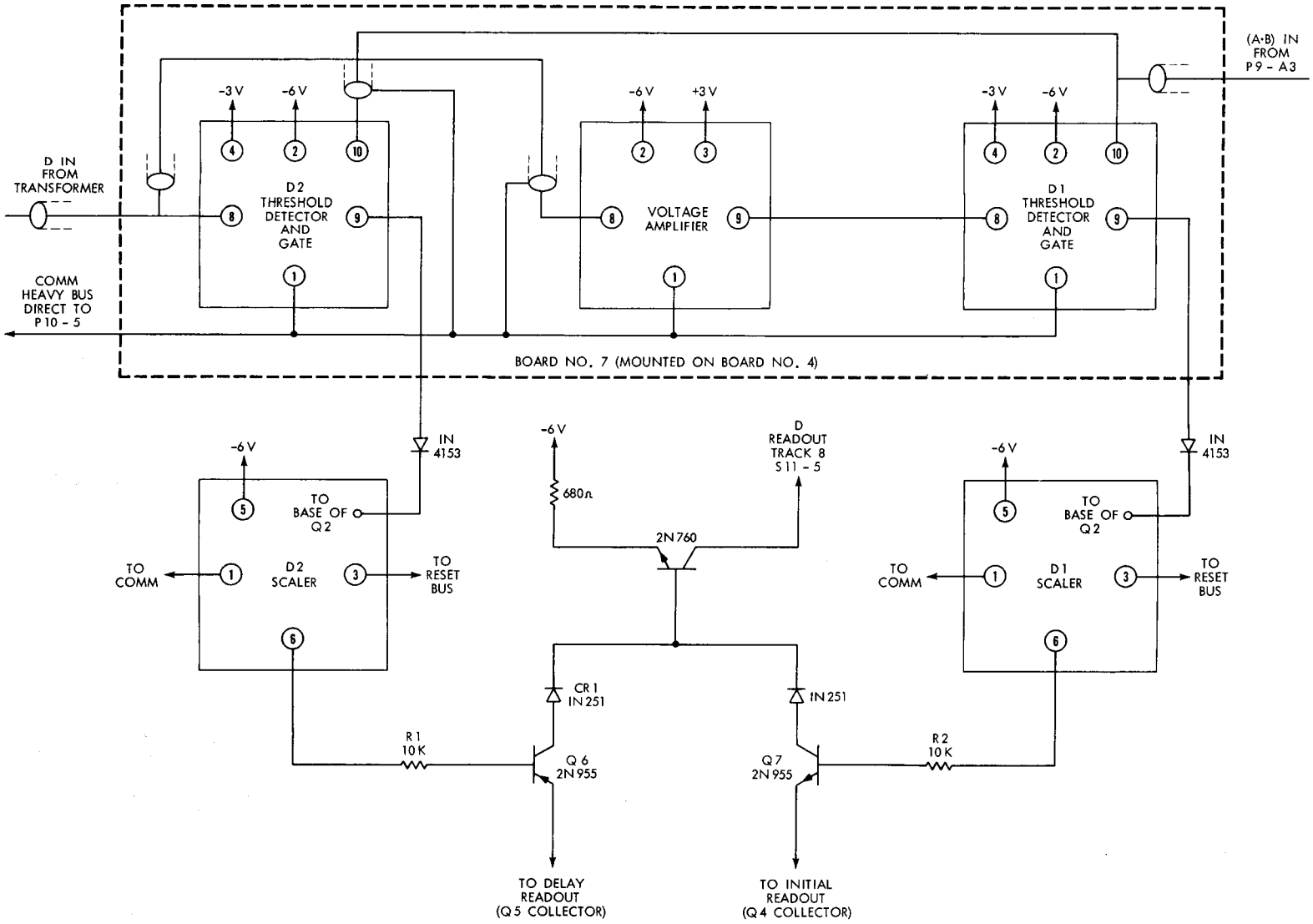


Figure 2. ADCR Mark 9 Board No. 7 and Modifications to Board No. 4.

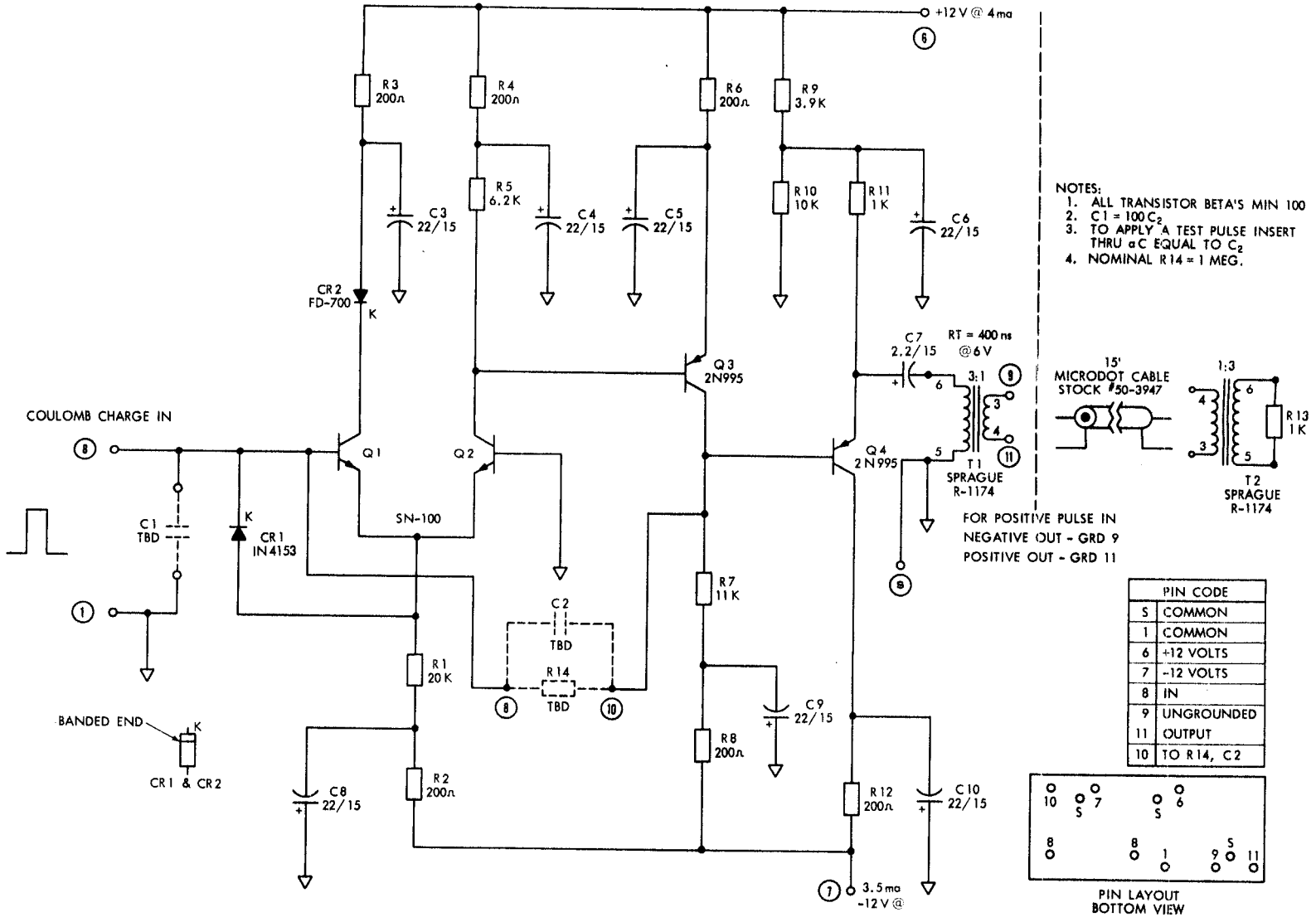


Figure 3. Charge Amplifier.

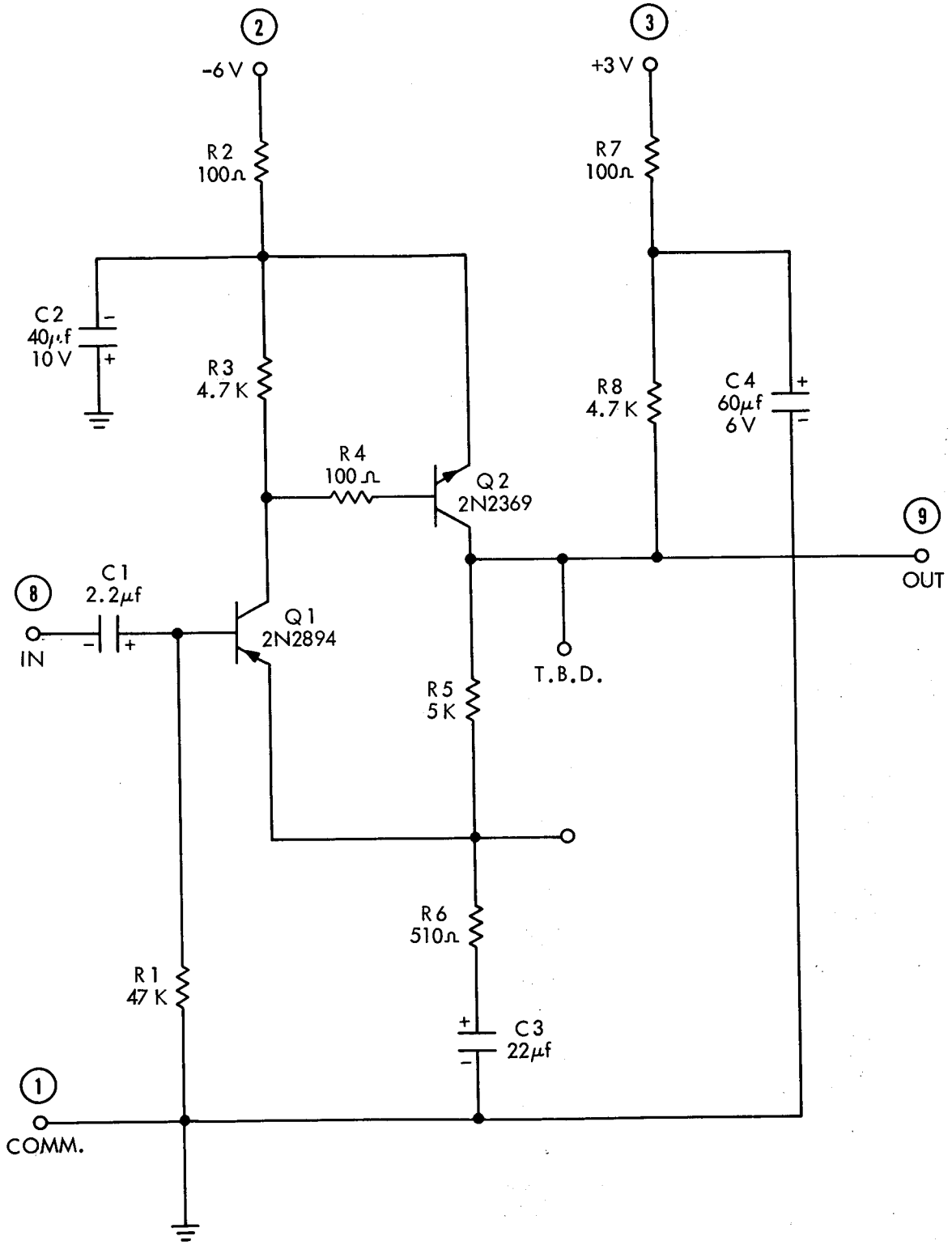
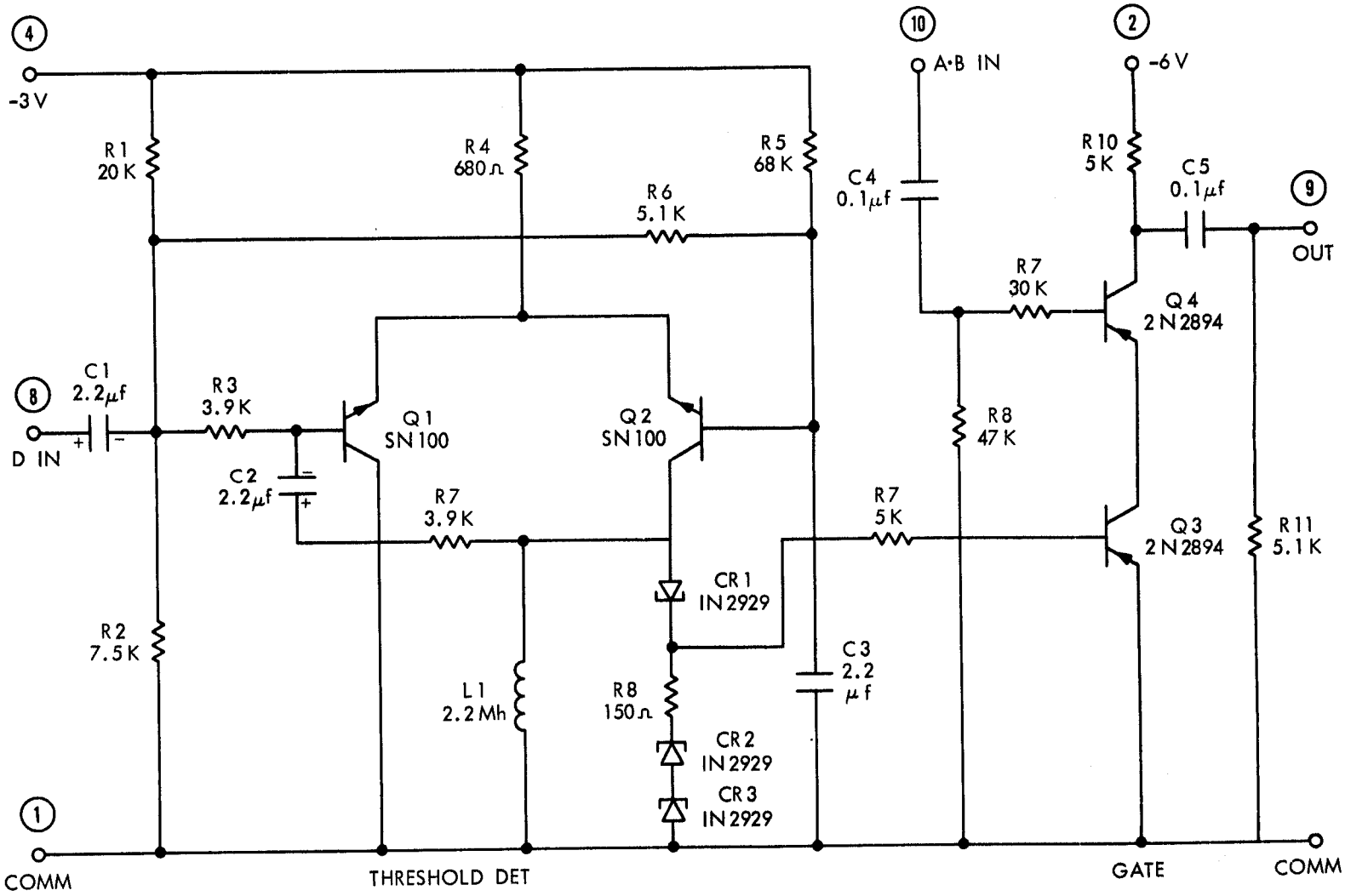


Figure 4. Voltage Amplifier.



Q1 & Q2 - B's at 1μa Ib & 0.5 V VCE <100 & MATCHED WITHIN 5

Q3 & Q4 - B's at 1μa Ib & 0.5 V VCE <15

Figure 5. Threshold Detector and Gate.

MODIFICATIONS TO MARK 6 CIRCUITS

The following modifications are made to convert the ADCR Mark 6 to an ADCR Mark 9 system:

A. Board No. 1 (See Figure 27, GSFC X-611-64-183)

1. Place transformer (Sprague R-1174) between input co-ax cable and input amplifier Type 1b in channels A, B, and C as shown in Figure 6.

B. Board No. 2 (see Figure 31, GSFC X-611-64-183)

1. Add single co-ax cable terminal connector P21.

2. Connect center conductor of a co-ax cable between P21 and the collector of the 2N929 transistor. Connect the shield of the cable to the common bus at the transistor end.

C. Board No. 4 (see Figure 33, GSFC X-611-64-183)

1. Mount the new board No. 7 on to board No. 4 as indicated in Figure 2.

2. Connect the +3v., -3v., -6v., and common terminals on board No. 7 to the corresponding bus on Board No. 4.

3. Hook up D1 and D2 scalers (Figure 21, GSFC X-611-64-183) by connecting scaler terminal 5 to the -6v. bus, terminal 1 to the common bus and terminal 3 to the Reset bus.

4. Add CR1, Q6, Q7, R1 and R2 to the track 8 readout circuit as shown in Figure 2.

5. Add single co-ax cable terminal connector P20.

6. Place transformer (Sprague R-1174) between input co-ax cable from P20 and terminal 8 of the D2 threshold detector as shown in Figure 7.

7. Connect a co-ax cable from terminal P9-A3 to terminal 10 of the D1 threshold detector as shown in Figure 2.

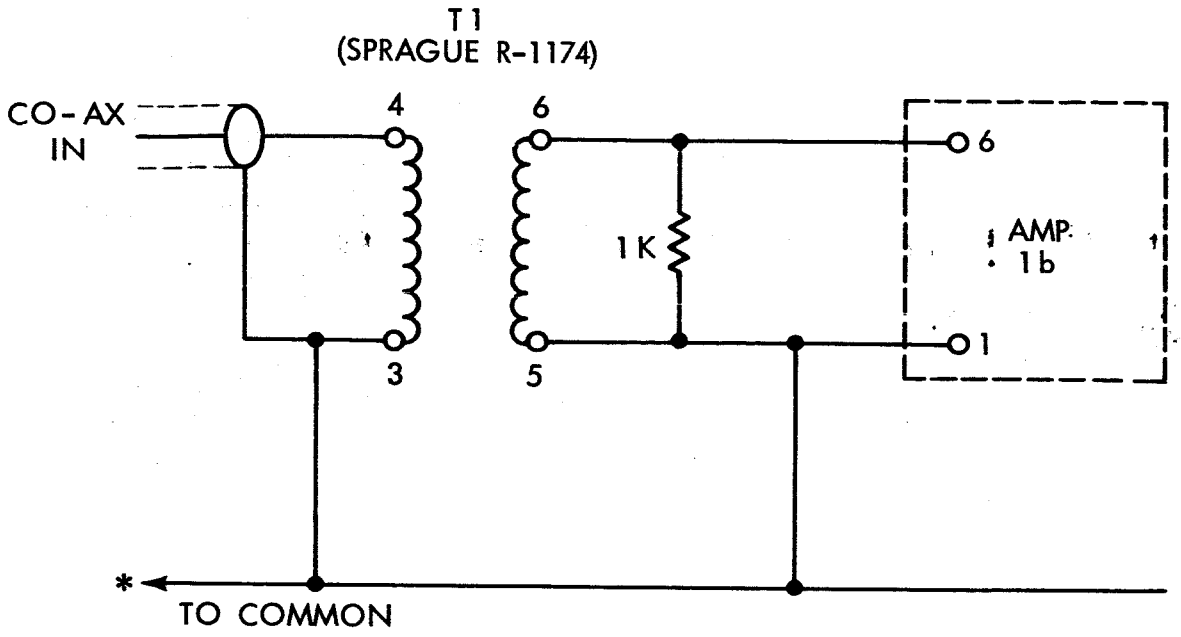


Figure 6. ADCR Mark 9, Board No. 1, Transformer and Connections for Channels A, B, and C.

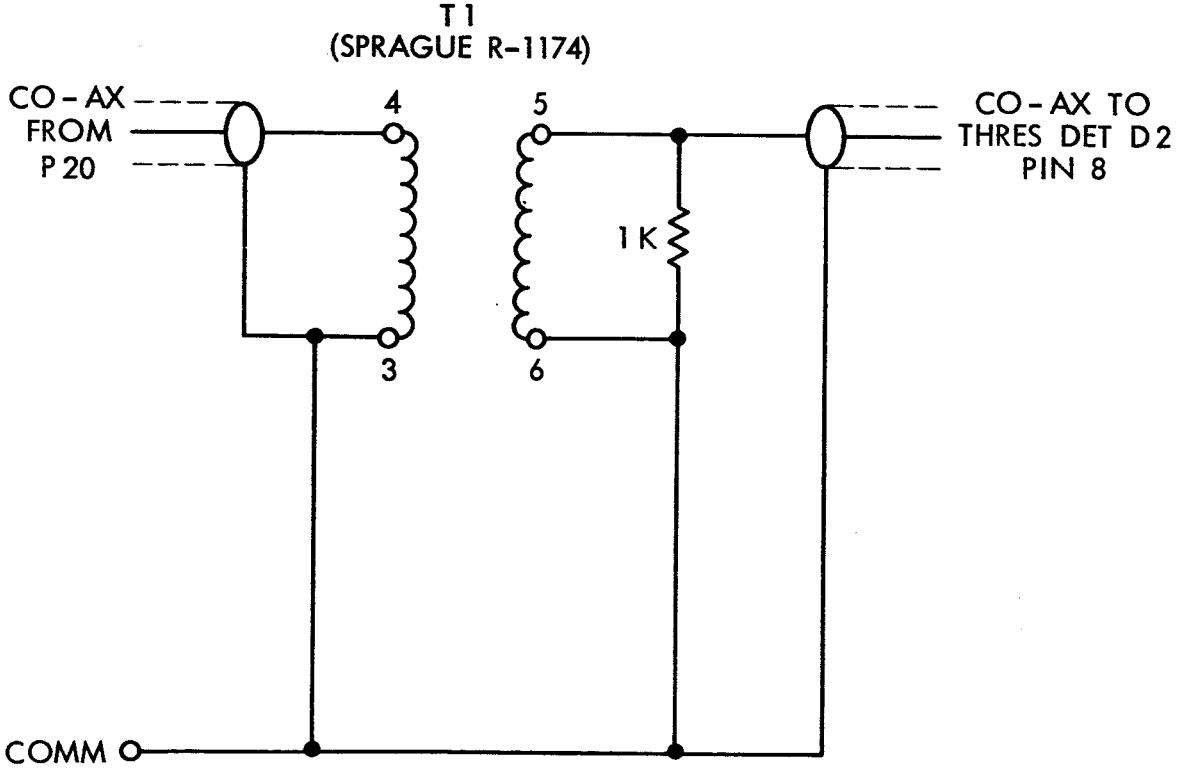


Figure 7. ADCR Mark 9, Board No. 4, Transformer and Connections for Channel D.

8. Connect terminal 9 on the D1 and D2 threshold detectors through diode 1N4153 to the base of Q2 (Figure 21, GSFC X-611-64-183) in the respective D1 and D2 scalers as shown in Figure 2.
9. Connect terminal 6 of scaler D1 through R2 to the base of Q7.
10. Connect terminal 6 of scaler D2 through R1 to the base of Q6.
11. Connect emitter of Q7 to the initial read bus.
12. Connect emitter of Q6 to the delay read bus.
13. Remove the 1N251 diode connected between the base of the 2N760 transistor in track 9 and the delay read bus.

D. Connect a co-ax cable between P21 on board 2 and P20 on board 4.

DIGITAL OUTPUT WORD FORMAT

Each time an event is processed in the ADCR Mark 9 system the readouts from channels A, B, C and D are recorded as two sixteen bit words on the 16 track magnetic tape. The information carried in each bit is as indicated in Table 1.

Table 1

ADCR MARK 6 DIGITAL OUTPUT WORD FORMAT

Track Number	Initial Readout	Delayed Readout
1	Bit A1	Bit B1
2	Bit A2	Bit B2
3	Bit A3	Bit B3
4	Bit A4	Bit B4
5	Bit A5	Bit B5
6	Bit A6	Bit B6
7	Bit A7	Bit B7
8	Bit D1	Bit D2
9	Index	No Output
10	Multiplier A1	Multiplier B1
11	Multiplier A2	Multiplier B2
12	Bit C1	Bit C6
13	Bit C2	Bit C7
14	Bit C3	Multiplier C1
15	Bit C4	Multiplier C2
16	Bit C5	Time Index